# Islanding of Grid-connected PV Inverters: Test Circuits and some Test Results

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**Abstract:** Many grid connected PV inverters are self-commutated. Therefore they have a certain design inherent tendency for islanding. For safety reasons islanding is a major concern of many utilities. Several different methods to prevent islanding are currently used. Passive monitoring of essential line parameters like voltage and frequency (in Japan often also harmonics) are not sufficient. Therefore also active methods (e.g. frequency shifting, continuous line impedance monitoring or power variations) are used. There are also many different proposals for tests circuits. The PV laboratory of HTA Burgdorf has carried out many islanding tests with different inverters and test circuits. In this paper some of these methods, their advantages and drawbacks and some test results are presented. At present there is no international consent how to prevent islanding of grid-connected inverters. However, at least a common test circuit seems feasible, where only one component has to be modified to perfom islanding test in countries requiring line impedance monitoring (e.g. Germany) or in countries that allow also other protecting schemes (e.g. frequency shifting).

**KEYWORDS: Grid-Connected - 1 : Inverter - 2 : Islanding - 3.**

## 1. Introduction

Many grid connected PV inverters are self-commutated, therefore they have a certain design inherent tendency for islanding. For safety reasons islanding is a major concern of many utilities.

In all the tests performed at the PV laboratory of HTA Burgdorf since 1988 on many inverters [1, 2, 3], islanding *never occurred after simply interrupting the connection to the mains*. The output voltage of the first inverters, which appeared on the Swiss market in the late eighties or early nineties and which had no RF filter on the AC side yet, dropped to 0 very quickly (within 1 or 2 cycles) after loss of line voltage. In newer inverters there are RF filters at the output to improve EMC behaviour. These filters represent a reactive load which tends to increase slightly the time until the cutoff of an inverter. Fig. 1 shows the output voltage of a newer inverter with an EMC filter after loss of line voltage under unmatched load conditions.

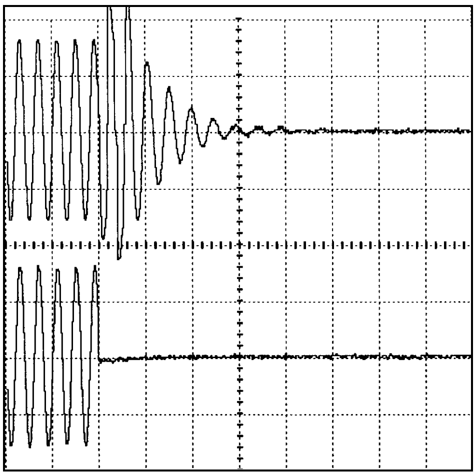

**Fig. 1: TopClass Grid II 4000/6, switch off *without matched load*, Pac ≈ 900W, no islanding.**

Top: output voltage of TC 4000/6 II, Bottom: line voltage, Vertical: 200V/div, Horizontal: 50ms/div.

After loss of line voltage, a considerable increase of voltage occurs for about 2 cycles.

## 2. Islanding under matched load conditions

*To provoke islanding, it was always necessary to match a load* at least to the real power of the inverter in order to bring the current between the inverter/load combination and the mains close to 0 before opening the connection switch. Self commutated inverters with RF-transformers usually have a power factor close to 1, therefore operation with matched real power was already sufficient to provoke islanding in most cases, especially with designs from new, unexperienced manufacturers. Fig. 2 shows the test circuit used for the first islanding tests. Fig. 3 shows islanding of an older inverter (SI-3000) after loss of line voltage.

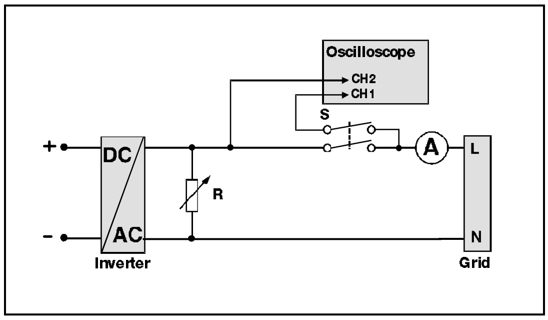


**Fig. 2: First test circuit for islanding tests with matched load.** Before opening the switches, R is adjusted to bring the current through ammeter A to a minimum. CH1 is used to determine the switching moment.

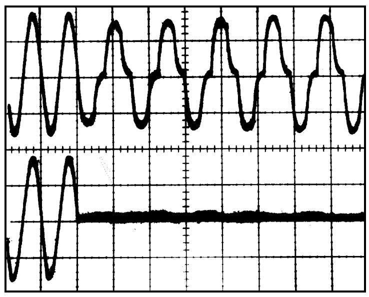

**Fig. 3: Islanding of SI3000 at Pac ≈ 420W, matched load in circuit of fig. 2.**

Top: output voltage of SI3000, Bottom: line voltage, Vertical: 200V/div, Horizontal: 20ms/div.

Islanding frequency is considerably lower and THD of voltage higher than under normal operating conditions.

In most cases, such an islanding problem could be cured very quickly by the manufacturer. Inverters with a microprocessor control usually solved this problem by a software modification.

For instance the stand alone frequency of the inverter can be chosen slightly higher or lower than the permitted frequency interval of the utility grid (in Europe: about 49.8 Hz to 50.2 Hz). By continuous monitoring of the output frequency by the microprocessor, an islanding condition can usually be detected easily within a reasonable time (less than 1 second). This frequency shifting scheme for islanding prevention is therefore quite easy to implement. To avoid problems in areas with high inverter penetration and inverters from different manufacturers, the *direction of the frequency shift and the permissible frequency interval under islanding conditions* (outside the normal mains frequency interval) should be prescribed by an internal standard.

With the upcome of newer inverter designs with low frequency ring-core transformers, which proved to be more rugged in practical operation, a certain amount of reactive power is drawn from the grid. Therefore it became necessary to include means to compensate any reactive power consumption of the inverter to improve the matching to the load during the test. A new German proposal for islanding tests also introduced a mains simulation resonance circuit with an additional L and C consuming a reactive power of ±100 Var (see fig. 4).

These measures make detection of an islanding condition more difficult for the inverter under test. Therefore the test circuit for the islanding tests used at the PV laboratory of HTA Burgdorf was modified to the circuit shown in Fig. 4. Fig. 5 shows an islanding test performed using this circuit with a newer inverter.

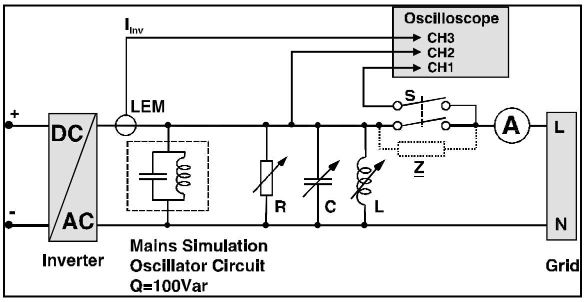


**Fig. 4: Improved test circuit for islanding tests.** R, L and C are adjusted until indication of ammeter A is at a minimum (ideal case: 0). For tests according to Swiss regulations Z is ∞. For tests according to the new German proposal, Z and mains impedance $\underline{Z}_M$ combine to the total impedance required for the test.

A three phase version of the test circuit of fig. 4 can be used for islanding tests of three phase inverters.

With the addition of an impedance Z accross the disconnect switch, the test circuit of fig. 4 becomes equivalent to the more complicated test circuit according to a new proposal from Germany, but it is much easier to realize and to handle than the original German circuit described in fig. 6.

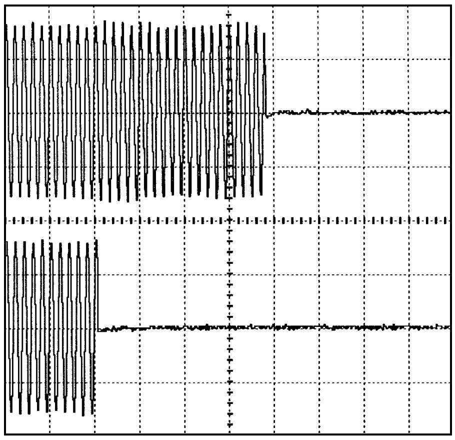

**Fig. 5: Solarmax S, loss of line voltage *with matched load*, Pac ≈ 800W, no islanding.**

Top: Output voltage of Solarmax S, Bottom: Line voltage, Vertical: 200V/div, Horizontal: 100ms/div.
About 380 ms after loss of line voltage the inverter shuts down. This time is considerably lower than the maximum time of 5 s permitted in the actual Swiss regulation.

## 3. Short description of some applicable regulations for islanding prevention

Due to space limitations, only the *key requirements* can be given here. Of course there are other requirements like disconnection under over- und undervoltage conditions, permissible frequency intervals and so on.

In **Switzerland** a very open regulation is applied:
*5 seconds after loss of line voltage the inverter must have switched off* under all load conditions (including matched load). This principal requirement must be fulfilled by single phase and three phase inverters. The method to be used is not specified.

In **Germany**, there are two different, more specific regulations for single phase inverters:

One possibility is the *use of a special three phase relay* in the inverter, permitting connection to the mains only if all three phases are active. As in case of a utility disconnection all three phases are disabled simultaneously, this measure is usually sufficient to avoid islanding problems, especially if the inverter itself also has some built in properties to prevent islanding.
The other, more recent proposal is to *monitor grid impedance to detect islanding*. The inverter must not connect the inverter if mains impedance $Z_M$ > 1.25 Ω. It must disconnnect the inverter within 5 seconds after a change $\Delta Z_M$ > 0.5 Ω or if $Z_M$ >1.75 Ω. Line impedance monitoring can be done efficiently in strong grids like in cities, but might cause problems in weak rural grids. To test line impedance at regular intervals, the inverters must change the injected current into the grid at regular intervals, calculate the line impedance from these measurements, update the stored values from previous measurements and compare changes and absolute values against the figures given in the regulation. If the current of the inverter itself is used, line impedance monitoring can be done only when a sufficient amount of power is injected into the grid. Fig. 6 shows the proposed test circuit.

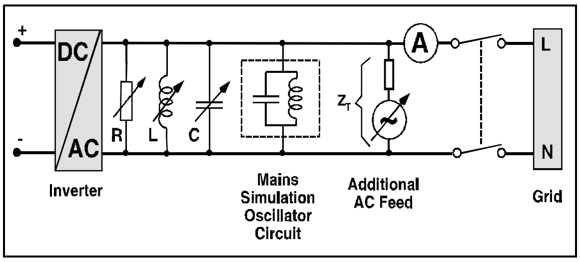


**Fig. 6: Circuit to test the automatic isolation according to new German regulation [4].**

Mains simulation oscillator circuit: An inductor L and a capacitor C consuming Q = ±100 Var. Additional AC feed: 30% of inverter power.

By means of some network theory this circuit can be be converted into the much simpler circuit of fig. 4 (use of equivalent voltage source). In fig. 7 the necessary steps are shown.

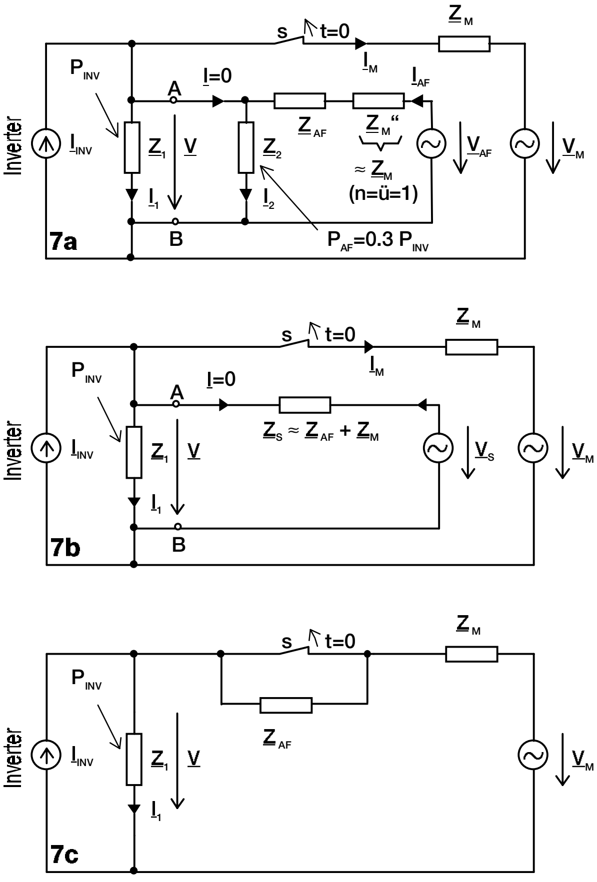


**Fig.7: Conversion of test circuit according to fig. 6 into test circuit of fig. 4.**

The mains is represented by a voltage source $\underline{V}_M$ in series with mains impedance $\underline{Z}_M$.

In fig. **7a**, total parallel impedance is split into $\underline{Z}_1$ taking real power $P_{INV}$ from the inverter and $\underline{Z}_2$ taking the power from the additional AC feed **AF** (usually connected at the same point by means of an adjustable transformer with $\underline{Z}_{AF}$). Mains impedance on the secondary side of this transformer is $\underline{Z}_M'' \approx \underline{Z}_M$ , as n ≈ 1.

When the **matching condition** is met, $\underline{\mathbf{I}}_{\mathbf{M}}$ **and** $\underline{\mathbf{I}}$ **are 0**.
To get circuit **7b**, $\underline{V}_{AF}$ , $\underline{Z}_{AF}$ , $\underline{Z}_M''$ and $\underline{Z}_2$ are converted to an equivalent voltage source $\underline{V}_S$ in series with $\underline{Z}_S \approx \underline{Z}_{AF}+\underline{Z}_M$ . ( $Z_2 >> |\underline{Z}_{AF}+\underline{Z}_M''|$).

As $\underline{\mathbf{I}}_{\mathbf{M}}$ and $\underline{\mathbf{I}}$ are **0**, $\underline{\mathbf{V}}_{\mathbf{S}} = \underline{\mathbf{V}} = \underline{\mathbf{V}}_{\mathbf{M}}$ . When switch S is open, the mains is still connected via $\underline{Z}_S \approx \underline{Z}_{AF} + \underline{Z}_M$ instead of only $\underline{Z}_M$ .

When switch S is open, circuit 7b is equivalent to the circuit of fig. **7c**. This is the much simpler circuit of fig. 4 with $\underline{Z} < \infty$ . Opening switch S creates an impedance step $\underline{Z}_{AF}$ .

## 4. Measuring principle of two inverters with grid impedance monitoring

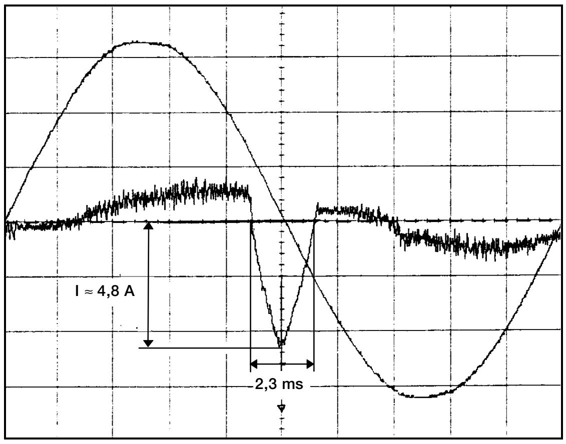


**Fig. 8: Grid impedance measuring of SMA SWR700, Pac ≈ 130W**

Curve 1: Output voltage of SWR700 (100V/div), Curve 2: Output Current of SWR700 (2A/div), Horizontal: 2ms/div.
A current peak close to the zero crossing of the line voltage is used.

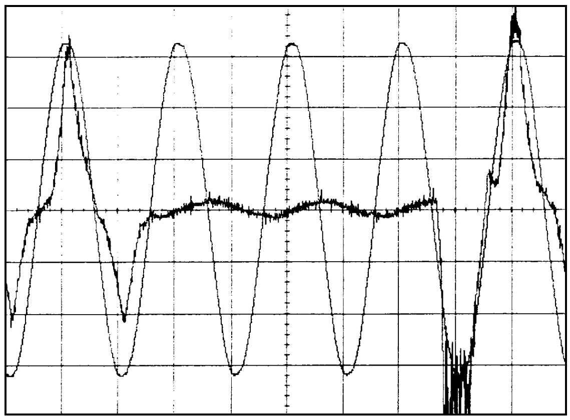

**Fig. 9: Grid impedance measuring of Siemens SPN1000 at Pac ≈ 130W**

Curve 1: Output voltage of SPN1000 (100V/div), Curve 2: Output Current of SPN1000 (2A/div), Horizontal: 10ms/div.
Injection of current (and power!) is interrupted for about 2.5 cycles. To get a big difference, a strong current pulse is used afterwards to measure line impedance.

## 5. Japanese test circuit

In a recent proposal from Japan [5], a similar islanding test circuit like fig. 4 (without a mains simulation oscillator circuit and with Z = ∞), but with the addition of an idling AC universal motor of about 500W is proposed. To get reproducable results, more information about the motor used (especially the moment of inertia and the rotating velocity) should be indicated.

## 6. Proposal for common islanding test circuit

As the German test circuit is equivalent to the circuit of fig. 4 with Z < ∞, a common test circuit for all islanding tests proposed in the last few years seems feasible by simple addition of the AC motor proposed by Japanese test institutions:

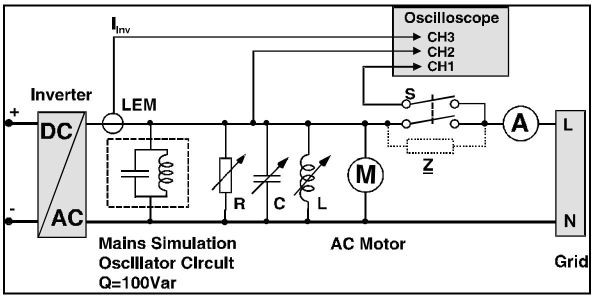


**Fig. 10:**
**Proposed common test circuit for islanding tests.**

For reproducable results, the type and rated power of the motor (e.g. universal AC motor or three phase AC induction motor operated single phase with a phase capacitor, S ≈ 500VA) and load conditions (idling, moment of inertia and rotating velocity) should be specified.

In countries where continuous impedance monitoring is required, values Z < ∞ can be applied, whereas in countries without impedance monitoring the circuit can be used with Z = ∞.

## 7. Conclusions

A simple method to detect islanding is to choose the free running frequency of the inverter outside of the frequency interval of the utility grid. By continuous monitoring of the inverter output frequency by the microprocessor, an islanding condition can be detected easily. This frequency shifting scheme is not affected by weak grids with relative high impedances in rural areas and does not require a minimum power level to be implemented practically. This method has been adopted by many manufacturers yet and is performing well in the field.

However, if this scheme is used, it is essential to standardize the direction of the frequency shift and the permissible frequency interval under islanding conditions (outside the normal mains frequency interval) in order to avoid problems in areas with high inverter penetration and inverters from different manufacturers.

Continuous line impedance monitoring is certainly a new and interesting approach to the problem of islanding prevention. However, it creates also some problems that need further consideration:

- If the operating current of the inverter itself is used, a certain minimum current (or power) is required to get a detectable impedance signal. Therefore, the test procedure used in Germany requires tests only at 30% and 100% of rated power. However, if islanding is a problem, it is not only dangerous at these power levels, but also at lower power levels and should be prevented also there.
- Continous current variations of inverters in order to measure mains impedance create additional noise (voltage fluctuations) on the mains which is certainly not desirable and reduces power quality. Current test pulses with *line frequency* are preferable to minimize possible interference.
- At locations with weak grids or frequent voltage fluctuations, stable operation of inverters with continuous line impedance monitoring may be affected or even be impossible.
- If a large number of inverters using line impedance monitoring is used close together, their test signals may interfere, giving false impedance values and make proper operation impossible.
- In cities with very large transformers, remaining loads in a disconnected part of the grid might constitute a total impedance lower than 0.5Ω preventing a detection of an islanding condition. This of course would only be a problem with a very large penetration of grid connected PV systems, which is not the case yet in the near future.

## Acknowledgements

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